

## AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions, and listings, of claims in the Application.

1-15 Canceled

16. (currently amended) A memory unit comprising:

a non-volatile memory including a protected area, the protected area further including an authorization unit information block and an authorization unit information block pointer;

a JTAG interface;

authorization logic configured to authorize software to run on a CPU based on secret information in the authorization unit information block; and

a controller configured to allow JTAG hardware to write information into the authorization unit information block and into the authorization unit information block pointer of said the protected area through said the JTAG interface, and to allow said the authorization logic exclusive access to read said the written information, said logic configured to authorize software to run on a CPU based on said written information and to prevent any over-writing of the written information until the non-volatile memory is entirely erased.

17. Canceled

18. (currently amended) The memory unit according to claim 16, further comprising a CPU interface clock generator for generating a system clock signal, the clock generator coupled to said the controller, wherein the clock generator, the non-volatile memory, the JTAG interface, the authorization logic and the controller are on a single chip.

19. (currently amended) The memory unit according to claim 18, wherein said the non-volatile memory includes an unprotected area, and said the controller allows said the

CPU to write, read and overwrite other information into ~~said~~ the unprotected area through ~~said~~ the CPU interface.

20. (currently amended) The memory unit according to claim 18, wherein ~~said~~ the controller allows ~~said~~ the CPU to write to ~~said~~ the non-volatile memory through ~~said~~ the CPU interface provided ~~said~~ the JTAG hardware is not writing to ~~said~~ the memory at the time.

21. (currently amended) The memory unit according to claim 20, wherein ~~said~~ the controller allows ~~said~~ the JTAG hardware to write to ~~said~~ the non-volatile memory through ~~said~~ the JTAG interface provided ~~said~~ the CPU has not issued a request to write to ~~said~~ the non-volatile memory at the time.

22. (currently amended) The memory unit according to claim 20, wherein ~~said~~ the CPU interface and ~~said~~ the JTAG interface are clocked by different clock signals and ~~said~~ the controller includes at least one synchronization buffer to synchronize communications received from ~~said~~ the CPU interface and ~~said~~ the JTAG interface.

23. (currently amended) The memory unit according to claim 22, wherein ~~said~~ the controller waits for a synchronization delay period related to ~~said~~ the at least one synchronization buffer before granting ~~said~~ the JTAG interface access to write to ~~said~~ the non-volatile memory, if ~~said~~ the CPU is not writing to ~~said~~ the non-volatile memory at a start of ~~said~~ the synchronization delay period and does not initiate a write to ~~said~~ the non-volatile memory before an end of ~~said~~ the synchronization delay period.

24. (currently amended) The memory unit according to claim 22, wherein ~~said~~ the at least one synchronization buffer includes:

a first buffer for synchronizing signals between ~~said~~ the JTAG interface and ~~said~~ the controller; and

a second buffer for synchronizing signals between ~~said~~ the CPU interface and ~~said~~ the controller.

25. (currently amended) A memory unit comprising:

a non-volatile memory including a protected area, the protected area further including an authorization unit information block and an authorization unit information block pointer;

authorization logic configured to authorize software to run on a CPU based on secret information in the authorization unit information block;

a JTAG interface clocked by a JTAG clock signal received from an external JTAG hardware; and

a controller configured to allow ~~said~~ the external JTAG hardware to write information into the authorization unit information block and into the authorization unit information block pointer of said the non-volatile memory through ~~said~~ the JTAG interface, and configured to allow the authorization logic exclusive access to read the written information, wherein ~~said~~ the controller is clocked ~~either~~ by a system clock signal if the system clock signal is available, and ~~or~~ by ~~said~~ the JTAG clock signal if ~~said~~ the system clock signal is not available.

26. Canceled

27. (currently amended) The memory unit according to claim 25, further comprising a CPU interface coupled to a CPU, wherein ~~said~~ the CPU is clocked by ~~said~~ the system clock signal, and ~~said~~ the controller is configured to allow ~~said~~ the CPU to write information into ~~said~~ the non-volatile memory through ~~said~~ the CPU interface provided ~~said~~ the external JTAG hardware is not writing to ~~said~~ the non-volatile memory at the time.

28. (currently amended) The memory unit according to claim 27, wherein ~~said~~ the system clock signal is generated in an integrated circuit chip that includes including said the JTAG interface, ~~said~~ the CPU interface, ~~said~~ the CPU, and ~~said~~ the controller; ~~and said JTAG clock signal is provided to said integrated circuit by said external JTAG hardware.~~

29. (currently amended) The memory unit according to claim 28, wherein ~~said~~ the controller includes a first synchronization buffer for synchronizing signals between ~~said~~ the JTAG interface and ~~said~~ the controller when ~~said~~ the controller is clocked by ~~said~~ the system clock signal.

30. (currently amended) The memory unit according to claim 29, wherein ~~said~~ the CPU interface is clocked by an IP-bus clock signal, and ~~said~~ the controller includes a second synchronization buffer for synchronizing signals between ~~said~~ the CPU interface and ~~said~~ the controller.

31. (currently amended) The memory unit according to claim 30, wherein ~~said~~ the controller waits for a synchronization delay period related to ~~said~~ the first and ~~said~~ the second synchronization buffers before granting ~~said~~ the JTAG interface access to write to ~~said~~ the memory, if ~~said~~ the CPU is performing a write to ~~said~~ the memory at a start of ~~said~~ the synchronization delay period and ~~said~~ the CPU does not initiate another write to ~~said~~ the memory before an end of ~~said~~ the synchronization delay period.

32-38 Canceled

39. (currently amended) The memory unit according to claim 16, wherein ~~said written information comprises an authorization unit information block and an authorization unit information block pointer, said authorization unit information block comprises secret information for authorizing said software, said~~ the authorization unit information block pointer is configured to specify an initial address of ~~said~~ the authorization unit information block, and ~~said~~ the authorization logic is further configured to lock ~~said~~ the software to ~~said~~ the CPU.

40. Canceled

41. (new) The memory unit according to claim 25, wherein the controller is configured to prevent any over-writing of the written information until the non-volatile memory is entirely erased.

42. (new) The memory unit according to claim 41, further comprising a clock generator for generating a system clock signal, the clock generator coupled to the controller, wherein the clock generator, the non-volatile memory, the JTAG interface, the authorization logic and the controller are on a single chip.

43. (new) The memory unit according to claim 42, wherein, when data is written into the authorization unit information block and into the authorization unit information block pointer through the JTAG interface while the clock generator is operating, signals from the external JTAG hardware are synchronized with signals in the controller by clocking the signals from the external JTAG hardware into a first input buffer using the JTAG clock signal and clocking the signals out of the first input buffer using the system clock signal.

44. (new) The memory unit according to claim 42, wherein the authorization unit information block pointer is configured to specify an initial address of the authorization unit information block, and the authorization logic is further configured to lock the software to the CPU.